U.S. Department of Commerce, Patent and Trademark Office	Application No.: 09/654,643
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Filing date: September 5, 2000
	Inventors: Pak Shing Chau et al.
LOW-LATENCY EQUALIZATION IN MULTI-LEVEL, MULTI-LINE COMMUNICATION SYSTEMS	Group Art Unit:
	Examiner name:
	Attorney Docket No. RA-19

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date, If Appropriate
EB	AA	5,539,774	7/23/96	Nobakht et al.	375	232	—
"	AB	5,596,439	1/21/97	Dankberg et al.	359	161	—
"	AC	5,608,755	3/4/97	Rakib	375	219	—
"	AD	5,694,424	12/2/97	Ariyavisitakul	375	233	—
"	AE	5,742,591	4/21/98	Himayat et al.	370	286	—
"	AF	5,809,033	9/15/98	Turner et al.	370	522	—
"	AG	5,887,032	3/23/99	Cioffi	375	257	—
"	AH	5,970,088	10/19/99	Chen	375	222	—
"	AI	5,982,741	11/9/99	Ethier	370	201	—
"	AJ	6,009,120	12/28/99	Nobakht	375	229	—
"	AK	6,034,993	3/7/00	Norrel et al.	375	232	—

Foreign Patent Documents

							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AL							
	AM							
	AN							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EB	AO	IEEE Standard 802.3ab-1999, 802.3 Supplement, Local and Metropolitan Area Networks, July 26, 1999.
"	AP	802.3ab, A Tutorial Presentation, 63 pages, undated, believed by applicants to have been presented at an IEEE 802.3 working group meeting in March 1998.
"	AQ	How 1000BASE-T Works, Geoff Thompson, IEEE802.3 Plenary, 13 November 1997, Montreal PQ Canada, 8 pages.
"	AR	A differential Error Reference Adaptive Echo Canceller for Multilevel PAM Line Codes, Perez-Alvarez et al. 0-7803-3192-3/96 ©96 IEEE, pp. 1707-1710.

Examiner EB	Date Considered 9/15/03

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

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LOW-LATENCY EQUALIZATION IN MULTI-LEVEL, MULTI-LINE COMMUNICATION SYSTEMS	Group Art Unit:
	Examiner name:
	Attorney Docket No. RA-19[illegible]

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date, If Appropriate
E.A	AA	6,067,319	5/23/00	Copeland	375	232	—
"	AB	6,101,223	8/8/00	Betts	375	261	—
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						

Foreign Patent Documents

							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AL							
	AM							
	AN							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

E.A	AO	A Gigabit Transceiver Chip Set for UTP CAT6 Cables in Digital CMOS Technology, Azadet et al., 2000 IEEE International Solid State Circuits Conference, pp. 306-307.
E.A	AP	A Scalable 32Gb/s Parallel Data Transceiver with On-chip Timing Calibration Circuits, Yang et al., 2000 IEEE International Solid State Circuits Conference, pp. 258-259.
"	AQ	Modulation schemes for high bit rate data transmission in the loop plant, URL-http://www.bib.fh-lippe.de/volltext/dipl/schlegel/chapter4.html, 29 pages, printed 4/19/01.
	AR	

Examiner [signature]	Date Considered 9/15/05

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U.S. Department of Commerce, Patent and Trademark Office	Application No.: 09/654,643
	Filing date: September 5, 2000
SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Inventors: Pak Shing Chau et al.
	Group Art Unit: 2631
LOW-LATENCY EQUALIZATION IN MULTI-LEVEL, MULTI-LINE COMMUNICATION SYSTEMS	Examiner name:
	Attorney Docket No. RA-194

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date, If Appropriate
EB	AA	5,295,157	03/15/94	Suzuki et al.	375	11	
"	AB	5,917,856	06/29/99	Torsti	375	231	
"	AC	6,061,395	05/09/00	Tonami	375	232	
"	AD	6,222,380	04/24/01	Gerowitz et al.	326	38	
"	AE	09/770,406	08/02/01	Hedburg	—	—	01/29/01
"	AF	09/745,988	08/23/01	Bonneau et al.	—	—	12/21/00
"	AG	09/858,760	09/06/01	Azazzi et al.	—	—	05/15/01
"	AH	09/201,114	09/11/01	Hasegawa et al.	—	—	09/11/01
"	AI	09/795,811	09/13/01	Govindarajan et al.	—	—	09/13/01
"	AJ						
	AK						

Foreign Patent Documents

							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AL							
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	AN							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EB	AO	Kuczynski et al., "A 1 Mb/s Digital Subscriber Line Transceiver Signal Proccesser", 1993 IEEE International Solid State Circuit Conference.
"	AP	S. D. Cova et al., "Characterization of Individual Weights in Transversal Filters and Application to CCD's" IEEE Journal of Solid-State Circuits, Vol. SC-17, No.6, December 1982.
"	AQ	Dally et al., "Multi-Gigabit Signaling with CMOS", May 12, 1997.
"	AR	A. Fiedler et al., "A 1.0625Gbps Transceiver with 2x-Oversampling and Transmit Signal Pre-Emphasis", 1997 IEEE International Solid State Circuit Conference and Slideset.

Examiner EB	Date Considered 9/15/03

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